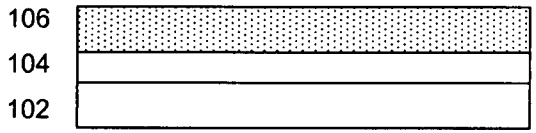
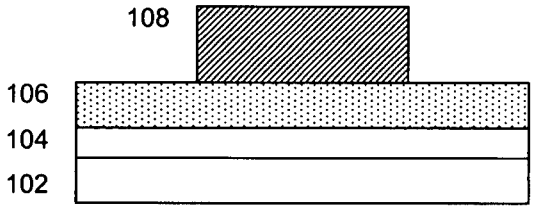
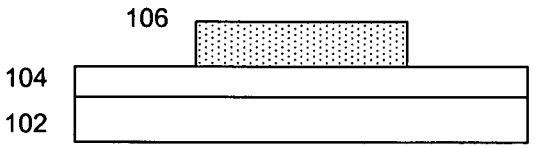
Fig, 1A



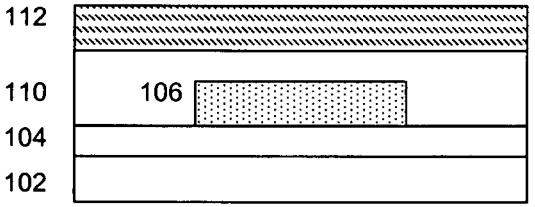
Fig, 1B



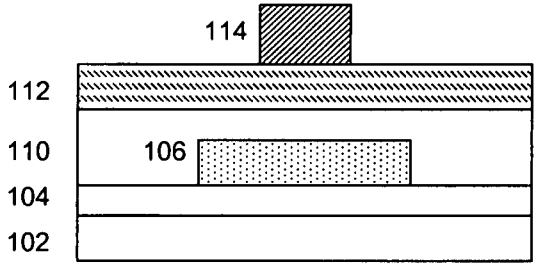
Fig, 1C



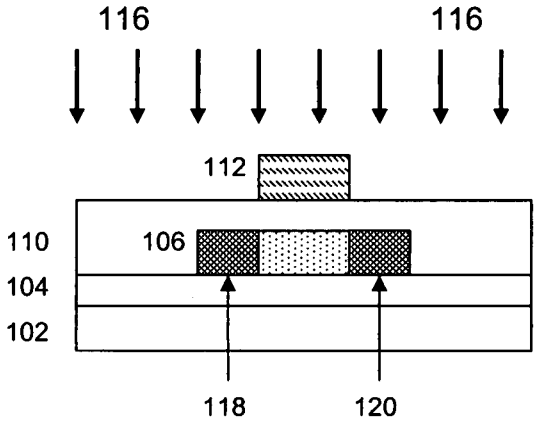
Fig, 1D



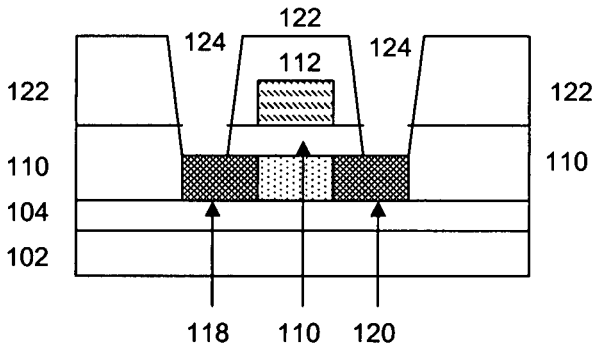
Fig, 1E



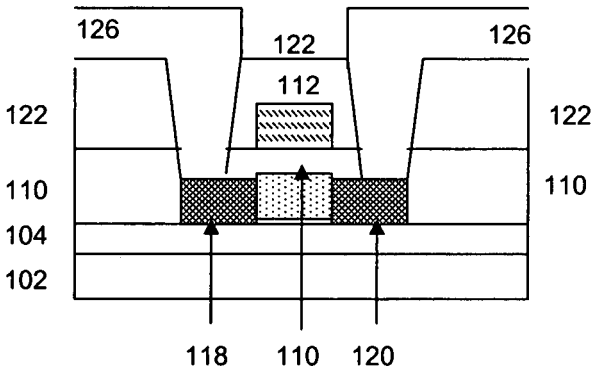
Fig, 1F



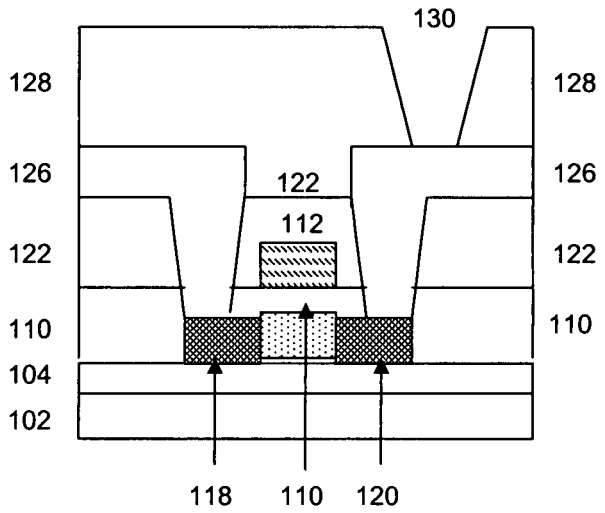
Fig, 1G



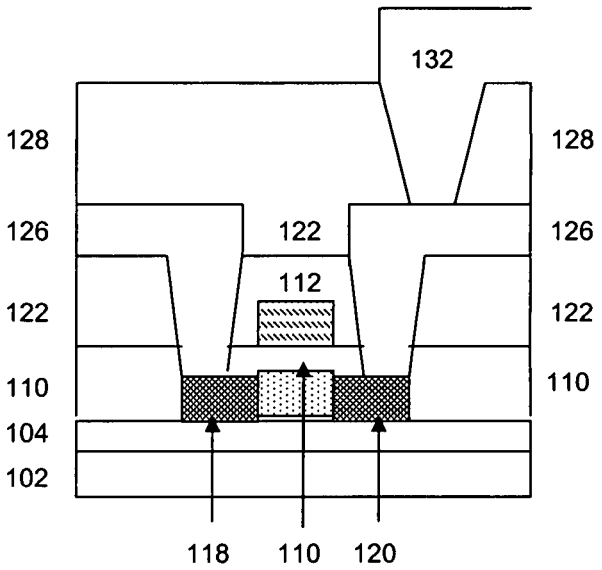
Fig, 1H



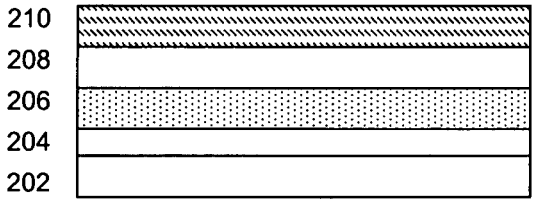
Fig, 1I



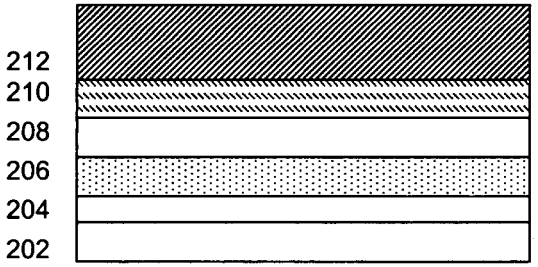
Fig, 1J



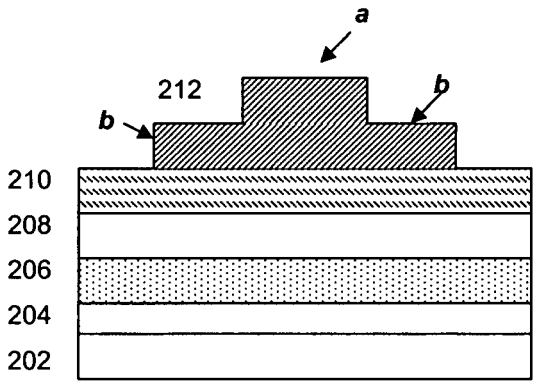
Fig, 2A



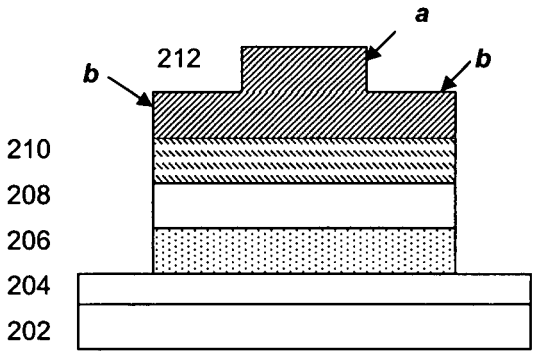
Fig, 2B



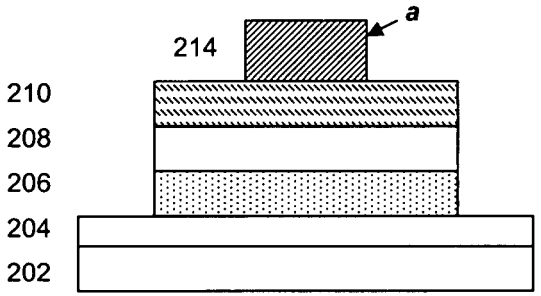
Fig, 2C



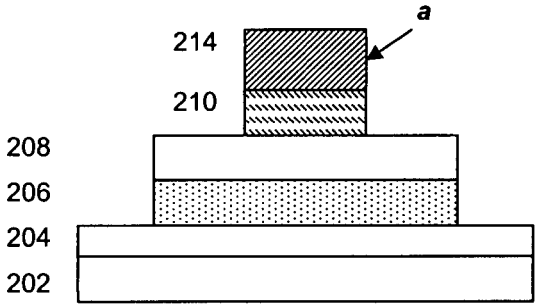
Fig, 2D



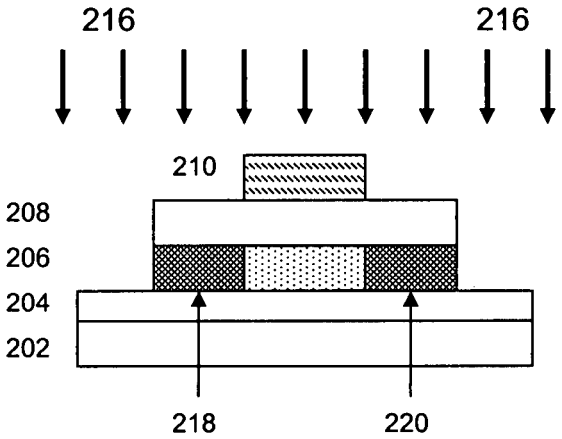
Fig, 2E



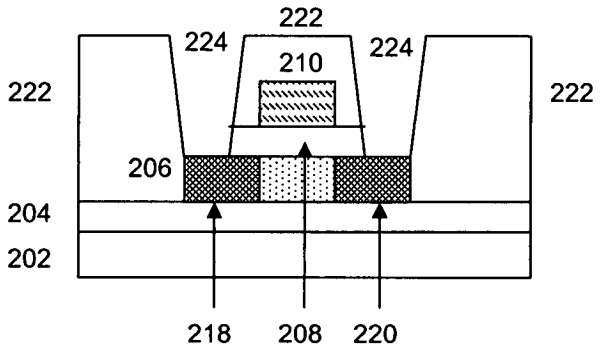
Fig, 2F



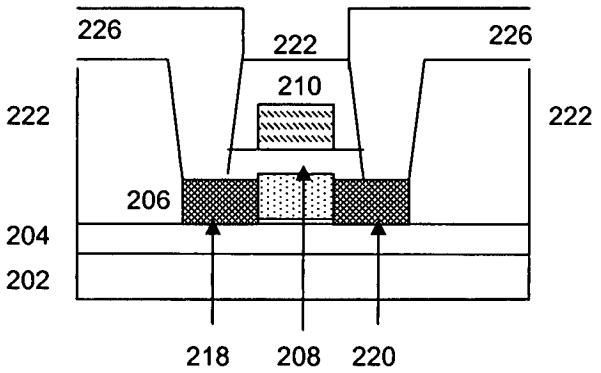
Fig, 2G



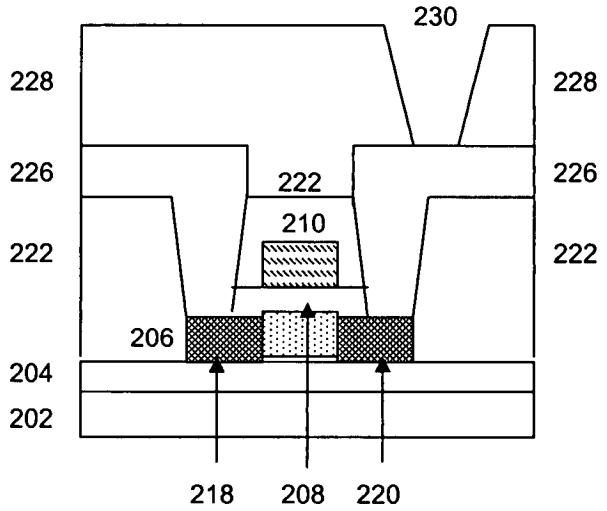
Fig, 2H



Fig, 2I



Fig, 2J



Fig, 2K

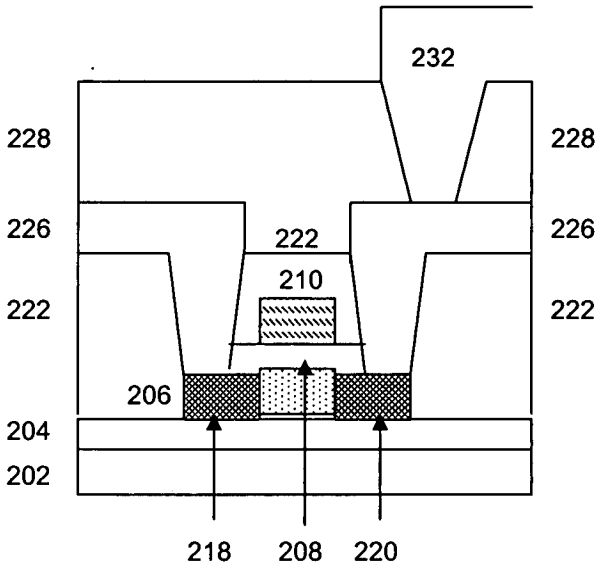
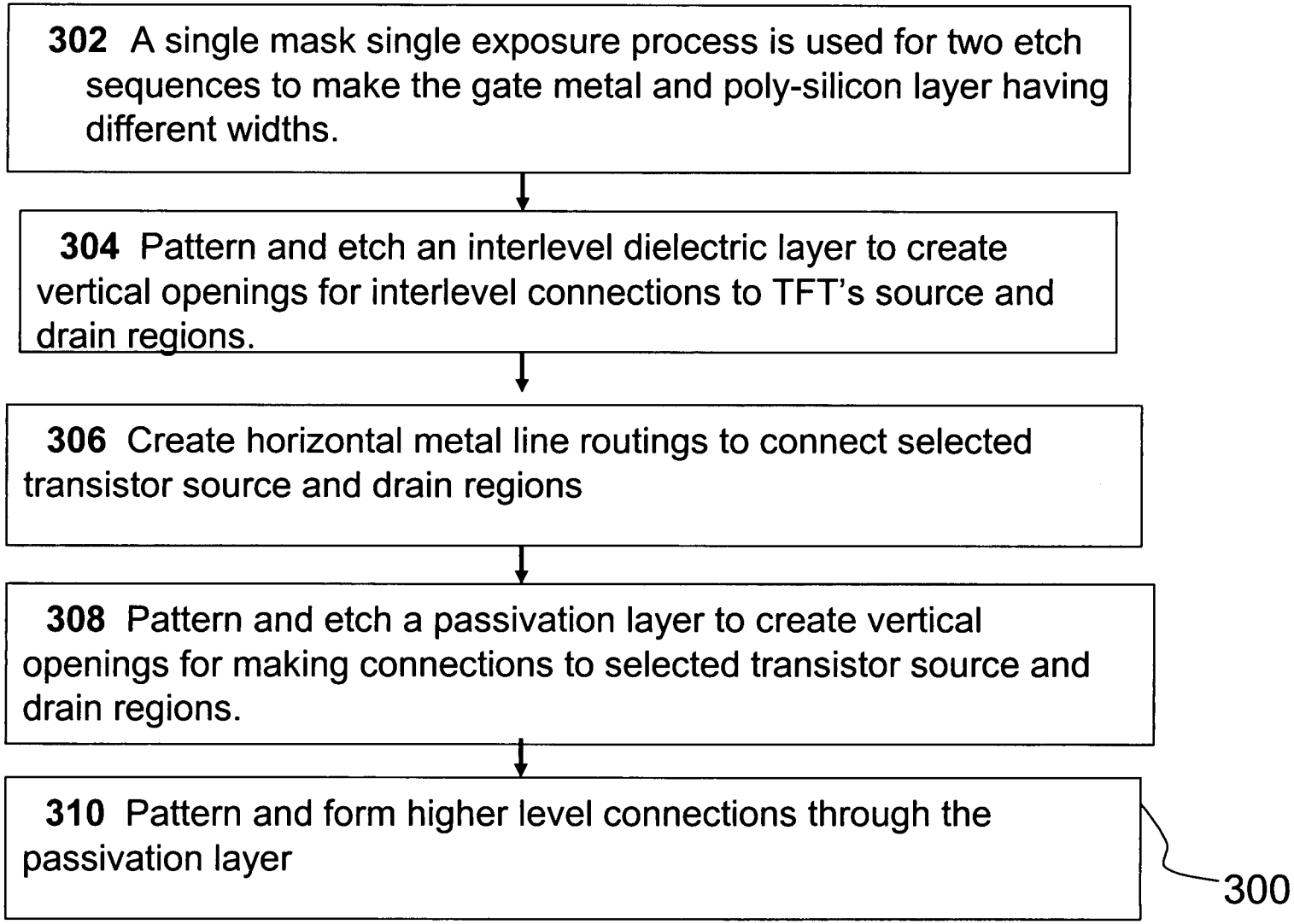


Fig. 3


302 A single mask single exposure process is used for two etch sequences to make the gate metal and poly-silicon layer having different widths.
304 Pattern and etch an interlevel dielectric layer to create vertical openings for interlevel connections to TFT's source and drain regions.
306 Create horizontal metal line routings to connect selected transistor source and drain regions
308 Pattern and etch a passivation layer to create vertical openings for making connections to selected transistor source and drain regions.
310 Pattern and form higher level connections through the passivation layer
300